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09/589,338	06/07/2000	John G. Rohrbaugh	10003687-1	8717

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,338	ROHRBAUGH ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on th cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. In view of the corrections made to the Abstract and Specification in Amendment B of Paper No.11 filed 11 July 2003, the Examiner withdraws all objections to the Abstract and Specification.

Claim Rejections - 35 USC § 112

2. In view of the corrections made to the Claims in Amendment B of Paper No.11 filed 11 July 2003, the Examiner withdraws all previous 35 USC § 112 rejections to the Claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 cites, "setting a plurality of the unspecified bit positions in accordance with a random filling methodology". The Examiner asserts that it is impossible for the unspecified bit positions to be filled using a random filling methodology since claim 1 requires that the specified bit positions be filled using a non-random filling methodology.

4. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 cite "using an algorithm that is conducive to compression". From the language, it is not clear whether the algorithm includes compression or not.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 8-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Chakradhar, Srimat T. et al. (US 5726996 A, hereafter referred to as Chakradhar).

35 U.S.C. 102(b) rejection of claim 1.

Chakradhar teaches a method for generating a set of test vectors for testing an integrated circuit (see Abstract and col. 3, lines 16-22, Chakradhar; Note: test sequence compaction is a method for generating a reduced set of test vectors or test sets for an

integrated circuit), each test vector of the set of test vectors containing a plurality of bits defining test inputs for the integrated circuit (col. 4, lines 23-26, Chakradhar; Note: in Chakradhar, a test vector is defined to be a set of logic values {**0**, **1**, or **X**} that are simultaneously applied to the primary inputs of the circuit), the method comprising the steps of: defining a list of faults for the integrated circuit (col. 11, lines 25-27, Chakradhar; Note: defining and using the non-essential faults of test sequence T_i as the target fault list is a step for defining the target fault list); generating at least one test vector that defines values for those inputs necessary to detect at least one target fault selected from the list of faults (col. 6, lines 25-31, Chakradhar; Note: Chakradhar teaches the generation of an extended test vector to detect a particular fault, hence, Chakradhar teaches generating at least one test vector that defines values for those inputs necessary to detect at least one target fault selected from the list of faults), the values comprising only a portion of the bits of the at least one test vector, wherein a remainder of the bits in the at least one test vector are unspecified bit positions (col. 4, lines 24-27, Chakradhar, Note: Chakradhar teaches that the value of the test vectors for a give test sequence consist of specified values **1** or **0** as well as unspecified values denoted with an **X**); and setting the values of a plurality of the unspecified bit positions using a non-random filling methodology (col. 10, lines 14-16, Chakradhar, Note: Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology).

35 U.S.C. 102(b) rejection of claim 8.

Chakradhar teaches adding a first test vector to a list of test vectors (in col. 6, lines 4-9, Chakradhar; Note: Chakradhar teaches producing, i.e., generating three initial test vectors, test vector **1** being a first test vector) and marking the selected fault as detected (in col. 6, lines 10-12, Chakradhar; Note: Chakradhar teaches that the first three test vectors detect essential faults, G6 s-a-1, G14 s-a-1, and G12 s-a-0, respectively whereby G6 s-a-1 corresponds to a fault that can be detected by the first test vector); generating an additional tests vector which defines values for those inputs necessary to detected a target fault selected from the list of faults, and other than one marked as detected (in col. 6, lines 19-21, Chakradhar; Note: Chakradhar teaches that an additional test vector is generated to detect the selected target fault, G2 s-a-0); determining whether the additional test vector may be compacted with any test vector in the list of test vectors (in col. 6, lines 22-31, Chakradhar; Note: Chakradhar teaches that the additional test vector can be compacted with test vector **1** if it is extended to detect essential fault, G6 s-a-1), and if so, compacting the additional test vector with a test vector in the set of test vectors, and if not, adding the additional test vector to the set of test vectors (in col. 6, lines 22-31, Chakradhar; Note: Chakradhar teaches that the additional test vector is compacted with test vector **1** to extend its fault detection capabilities and added to the set of test vectors; see also col. 5, lines 20-25, Chakradhar where Chakradhar explicitly states that if a test vector, which detects one or more essential faults, cannot be merged with another, it cannot be dropped hence even

if the additional vector cannot be compacted it must be added since none of the other test vectors can detect the selected target fault, G2 s-a-0).

35 U.S.C. 102(b) rejection of claim 9.

In col. 6, lines 10-12, Chakradhar teaches that test vector **1** detects three essential faults: G6 s-a-1, G7 s-a-0 and G14→G10 s-a-0.

35 U.S.C. 102(b) rejection of claim 10.

In col. 6, lines 10-12, Chakradhar teaches that test vectors 1, 2 and 3 detect essential faults G6 s-a-1, G14 s-a-1, and G12 s-a-0, respectively.

35 U.S.C. 102(b) rejection of claim 11.

In col. 6, lines 10-12, Chakradhar teaches that test vector **1** detects the essential fault, G6 s-a-1.

35 U.S.C. 102(b) rejection of claim 14.

In col. 22, lines 53-67, Chakradhar teaches that outputs for the at least one test, vector are generated in response to the compacted condition.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-7, 12, 13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakradhar, Srimat T. et al. (US 5726996 A, hereafter referred to as Chakradhar).

35 U.S.C. 103(a) rejection of claim 2.

Chakradhar, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Chakradhar, does not explicitly teach the specific use of assigning the unspecified values to a value of one.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar; Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the

unspecified values to a value of one is a means and a specific embodiment for non-random assignment of the unspecified values.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chakradhar by including an additional step of assigning the unspecified values to a value of one. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that assigning the unspecified values to a value of one would have provided the opportunity to implement a specific embodiment for non-random assignment of the unspecified values as suggested in the Chakradhar patent.

35 U.S.C. 103(a) rejection of claim 3.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar, Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the unspecified values to a value of zero is a means and a specific embodiment for non-random assignment of the unspecified values.

35 U.S.C. 103(a) rejection of claims 4-7.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar, Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that

were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the unspecified values to specified values of zeros and ones is a means and a specific embodiment for non-random assignment of the unspecified values.

35 U.S.C. 103(a) rejection of claim 12.

In col. 6, lines 10-12, Chakradhar teaches that test vector **1** detects three essential faults: G6 s-a-1, G7 s-a-0 and G14→G10 s-a-0. In col. 6, lines 22-23, Chakradhar teaches the use of fault simulation.

35 U.S.C. 103(a) rejection of claim 13.

Testing a subset of the integrated circuit does not deviate from the scope or the intent of the teachings in the Chakradhar patent since a subset of the integrated circuit is still an integrated circuit.

35 U.S.C. 103(a) rejection of claim 15.

Claim 15 cites substantially the same limitations as in claim 1 except that it provides an apparatus for carrying out the method of claim 1, hence is rejected for the same reasons as in claim 1.

35 U.S.C. 103(a) rejection of claim 16.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar, Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the unspecified values to a value of one is a means and a specific embodiment for non-random assignment of the unspecified values.

35 U.S.C. 103(a) rejection of claim 17.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar, Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the unspecified values to a value of zero is a means and a specific embodiment for non-random assignment of the unspecified values.

35 U.S.C. 103(a) rejection of claims 18-20.

The Examiner asserts that in col. 10, lines 14-16, Chakradhar, Chakradhar teaches that the test generator does **not** randomly assign values to primary inputs and scan FFs that were left unspecified, hence Chakradhar teaches setting the values of a plurality of the unspecified bit positions using a non-random filling methodology. Assigning the unspecified values to specified values of zeros and ones is a means and a specific embodiment for non-random assignment of the unspecified values. Note: any

deterministic method for assigning values is conducive to compression since the algorithm can be repeated.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bershteyn, Mikhail (US 5485471 A) teaches partitioning of tailored test vectors into subsets and filling of the subsets with similar vectors starting with vectors close to the initially selected vector and continuing to add vectors farther away until an optimal number of vectors are in the subset. Hosokawa, Toshinori et al. (US 6253343 B1) teaches design for testability and test sequence generation for integrated circuits. S. T. Chakradhar et al, "A Transitive Closure Algorithm for Test Generation," IEEE Trans. on Computer-Aided Design, vol. 12, pp. 1015-1028, July 1993. TDB-ACC-NO: NN770647; "PLA Macro Optimized Test Pattern Generation"; IBM Technical Disclosure Bulletin, June 1977, Vol. 20, Isuue 1, Page No. 47-53.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres
July 19, 2003